REMARKS/ARGUMENTS

Claim 1 has been amended to more clearly indicate the amorphous silicon pattern comprises a first region, a second region, at least one first pointed region, a third region, and at least one fourth region. Claim 12 has been amended to replace the term "forming at least one patterned gate electrode on the gate insulating layer on each fourth region;" by "forming at least one patterned gate electrode on the gate insulating layer on each fourth region." to correct the grammar. Claims 19-25 are added to mention the gate electrode on the gate insulating layer formed on each fourth region, as Fig. 10 shows. No new matter is added.

1.Claims 1, 2, 7, 11 are rejected under 35 U.S.C. 103(a) as being anticipated by Ishida (US6,534,789 B2).

The reasons of record that can be found on page 2 in the Office action.

Response:

Claim 1 of the applicant's invention is noted a fourth height smaller than the second height. When the laser crystallization process performs, an amorphous silicon seed in each first pointed region adjacent to each fourth region to grow and to crystallize as a first single crystal silicon grain in each fourth region. The present invention uses this feature to produce the bigger single crystal silicon grain, the grain boundary decreases, the considerable grain boundary will not trap electrons flowing through the channel region to reduce the conductive current, and when the LTPS-TFT is turned off, electrons will be released to increase the leakage current.

But, Ishida (US6,534,789 B2) is related to a thin film transistor matrix having TFT with LDD regions. As shown in FIG. 1A, on the flat surface of a glass substrate 1, an

SiO.sub.2 layer 2 was deposited to a thickness of about 200 nm by plasma enhanced (PE) chemical vapor deposition (CVD) at a substrate temperature of about 300.degree., the SiO.sub.2 layer preventing impurities in the glass from being mixed with materials of other layers to be formed on the SiO.sub.2 layer. On this SiO.sub.2 layer 2, an amorphous Si layer 3 was deposited to a thickness of about 50 nm by CVD. Laser annealing was performed for the amorphous Si layer 3 to change it to a polysilicon layer 3 (Col 4, lines 21-31). Ishida lacks any suggestion that its amorphous Si layer can and should be modified in a manner required to meet the amorphous silicon pattern in independent claim 1.Figs. 1A-1D are noted the substrate was dipped in the TMAH aqueous solution 6 for about 60 seconds, and was washed with pure water and the surface of the metal layer 5 was dried. When the underlying metal layer 5 was wet-etched by using, the side wall 5s of the metal layer 5 was produced, and the side wall 5s has a constant forward or normal taper angle relative to the surface of an underlying layer (column 4, lines 41-67). Besides, the gate electrode 15 of Figs. 5A-5C is the same with the metal layer 5 of Figs. 1A-1D. The gate electrode 15 also has a side wall which has a taper angle relative to the surface of an underlying layer. When the ion implantation processed, the gate electrode 15 and the gate insulating film are as the mask for the ion implantation, the TFT will be formed a SLDD region 13c, a LDD region 13d, and a HDD region 13h (column 8, lines 4-38).

The applicant's invention is different form Ishida (US 6,534,789 B2). (1) Ishida (US6,534,789 B2) uses one uniform anamorphous silicon layer which was deposited to a thickness of about 50 nm by CVD. Even, repeats laser annealing process to form poly-silicon layers, Ishida (US 6,534,789 B2) still can't form a single crystal silicon grain. But, in the applicant's invention, two regions (the fourth region and the first pointed region) have different heights, after laser crystallization process, the fourth region could form a single crystal silicon grain. (2) Because the applicant's invention uses the heights of the fourth region and the first pointed region are different to course the different laser melting effects in the fourth region and the first pointed region. But Ishida (US6,534,789 B2) not use any

different heights to course any different melting effects. (3) If Ishida (US6,534,789 B2) can not use different heights to course any different melting effects. Ishida (US6,534,789 B2) can not form any amorphous silicon seed and single crystal silicon grain. So, even the person having ordinary skill in the art to understand Ishida (US6,534,789 B2), the applicant's invention still can not be made. Claim 1 of the applicant's invention is unobvious from Ishida (US6,534,789 B2) and is obtained by 35 U. S. C. 103 (a).

Claims 2, 7, 11 are patentably distinguishable from Ishida (US6,534,789 B2), because claim 1 is unobvious from Ishida (US6,534,789 B2). Reconsideration of the amended claims is politely requested.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

2. The Oath/Declaration has not been received with the instant application.

The record can be found on page 2 in the Office action.

Response:

The declaration can be found in the Image File Wrapper of PAIR system. Should this PAIR page prove inaccurate or the received document not be the declaration as requested, the applicant respectfully request additional notice so that this matter can be timely corrected.

The declaration is submitted again for examiner's convenience, but the late oath or declaration surcharge USD 130 should not be charged. And a timely Notice of Allowance is respectfully request.

Sincerely yours,

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Note: Please leave a message in my voice mail if you need to talk to me. (The time in D.C. is 12 hours behind the Taiwan time, i.e. 9 AM in D.C. = 9 PM in Taiwan.)